a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection between the first position and the position in the comparand.

Please add the following new claims:

49. (New) A content addressable memory (CAM) device, comprising:

means for receiving an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups;

means for translating, in response to first translation information, the first bit group from the first position to a different position in a comparand; and

means for comparing the comparand with data stored in a CAM array.

50. (New) The apparatus of claim 49, further comprising means for decoding the first translation information.

51. (New) The apparatus of claim 50, further comprising means for programming the CAM device with the first translation information.

52. (New) The apparatus of claim 49, wherein the input data has a second bit group having a second position in the input data relative to other bit groups and wherein the apparatus further comprises:

means for translating the second bit group from the second position to a second position of the comparand in response to second translation information.

53. (New) The apparatus of claim 52, further comprising means for concurrently translating the first and second bit groups into the comparand.

54. (New) The apparatus of claim 52, further comprising means for sequentially translating the first and second bit groups into the comparand.

55. (New) The apparatus of claim 54, further comprising means for selecting the first translation information in a first cycle and the second translation information in a second cycle.